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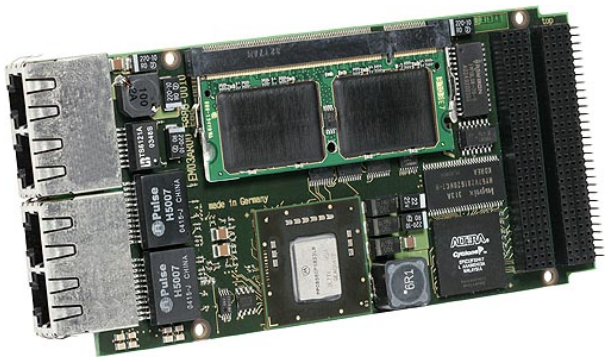
EM3 - Embedded System Module with MPC8560



- **MPC8560, 800 MHz**
- **FPGA 12,000 LEs (approx.144,000 gates)**
- **32-bit/33-MHz PCI, opt. 64-bit/66-MHz**
- **Up to 2 GB DDR SDRAM (SO-DIMM)**
- **NAND Flash**
- **2 Gigabit / 1 Fast Ethernet, 1 COM (RJ45)**
- **COMs, CAN, graphics, IDE etc. via FPGA**
- **Stackable with PCI-104**
- **MENMON™ BIOS for PowerPC® cards**

The EM3 is a complete embedded SBC for use on any carrier board in different industrial environments. The final application consists of a stand-alone EM3, an EM3 with an application-specific carrier card and/or with additional PCI-104 modules.

The EM3 is controlled by an 800-MHz MPC8560 integrated PowerPC® processor.
The EM3 is equipped with an on-board 133 MHz fast DDR RAM on an SO-DIMM socket for data and with NAND Flash for program storage. It provides front-panel access for two Gigabit Ethernet, one fast Ethernet and one COM via four RJ45 connectors. Additional functionality such as high-level telco protocols and other functions provided inside the MPC8560, as well as graphics, touch, CAN, protocol converters etc. can be realized in an FPGA for the needs of the individual application. The corresponding connectors are available on a carrier board. The functionality of the FPGA is dynamically loaded by the application software.
The EM3 comes with MENMON™ support. This firmware/BIOS can be used for bootstrapping operating systems (from disk, Flash or network), for hardware testing, or for debugging applications without running any operating system.
The EM3 is a communication engine ideal for use in routers, switches, base stations, as an embedded Linux server but also for high-end automation and robot control under a real-time operating system. It can be used in embedded applications and it also makes a perfect fit as a system controller in a 6U CPCI or VME environment - combined e.g. with PMC mezzanines.
For a first evaluation of the functions of the EM3 we strongly recommend to use the EK7 ESM™ starter kit. The kit consists of the standard CPU module EM8 (as EM3 but with MPC8540), an FPGA loaded with additional I/O functions, the carrier card with I/O connectors, an external PSU, cables, and an adapter for mounting a PCI-104 module.

ESM™ modules consist of the hardware (CPU, chip set, memory, I/O) which is not fixed to any application-specific function, and an FPGA programmed in VHDL code, which provides I/O that is also still independent of a specific application. ESM™ modules are based on PCI. They have two or three system connectors: J1 has a fixed signal assignment, while J2 is variable depending on the final application-specific configuration of the ESM™ and the carrier board. J2 also feeds the I/O signals of the functions programmed in the FPGA to the carrier card. Some ESM™ modules have an additional J3 connector that is used to replace the front I/O connectors to route the signals to the carrier board or to the backplane of a CPCI or VME system.

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Technical Data

CPU
- PowerPC®
  - MPC8560 PowerQUICC™ III
  - 800MHz (666..833MHz optional)
  - e500 PowerPC® core with SPE APU and MMU
  - Integrated Northbridge and Southbridge
  - High memory bandwidth

Memory
- 2x32KB L1 data and instruction cache, 256KB L2 cache / SRAM integrated in MPC8560
- Up to 2GB SDRAM system memory
  - One SO-DIMM slot for SDRAM modules
  - DDR2100 with or without ECC
  - 133MHz memory bus frequency
- Up to 1GB soldered NAND Flash (and more), FPGA-controlled
- Up to 16MB additional SDRAM, FPGA-controlled, e.g. for video data and NAND Flash firmware
- 8MB boot Flash
- 32KB non-volatile FRAM
- Serial EEPROM 4kbits for factory settings

Mass Storage
- Parallel IDE (PATA)
  - One port for hard-disk drives
  - Available via I/O connector
  - FPGA-controlled
- Up to 1GB soldered ATA NAND Flash (and more), FPGA-controlled

Graphics
- Available via I/O connector
- FPGA-controlled

I/O
- Three Ethernet channels
  - Two 10/100/1000Base-T Ethernet channels
  - One 10/100Base-T Ethernet channel
  - Three RJ45 connectors at front panel
  - Two onboard LEDs to signal LAN Link and Activity
- One RS232 UART (COM1)
  - One RJ45 connector at front panel
  - Data rates up to 115.2kbits/s
  - 16-byte transmit/receive buffer
  - Handshake lines: CTS, RTS
- Further I/O depending on FPGA configuration

Front Connections
- Three Ethernet (RJ45)
- One RS232 UART COM1 (RJ45)

FPGA
- Standard factory FPGA configuration:
  - Main bus interface
  - 16Z070_IDEDISK - IDE controller for NAND Flash
  - 16Z043_SDRAM - Additional SDRAM controller (16MB)
  - 16Z023_IDENHS - IDE controller (PIO mode 0; non-hot-swap)
  - 16Z044_DISP - Display controller (1024 x 768, 60Hz/70Hz, 6-bit RGB)
  - 16Z031_SPI - SPI touch panel controller
  - 16Z025_UART - UART controller (controls COM10..COM12)
  - 16Z034_GPIO - GPIO controller (8 lines)
- The FPGA offers the possibility to add customized I/O functionality. See FPGA.

PCI Interface
- 32- or 64-bit, 33-MHz PCI interface at PCI-104 connectors J1 and J2
- Compliant with PCI Specification 2.2
- Support of four external masters

Miscellaneous
- Real-time clock with GoldCap backup
- Power supervision and watchdog

Electrical Specifications
- Supply voltage/power consumption:
  - +5V (-2%/+5%), 2.5A
  - +3.3V (-2%/+5%), 0.5A
- MTBF: tbd. @ 40°C (derived from MIL-HDBK-217F)

Mechanical Specifications
- Dimensions: conforming to ESM™ specification (PCB: 149mm x 71mm), Type I-S
- Weight: 110g (w/o heat sink); standard heat sink: 155g

Environmental Specifications
- Temperature range (operation):
  - 0..+60°C
  - Airflow: min. 10m³/h
- Temperature range (storage): -40..+85°C
- Relative humidity (operation): max. 95% non-condensing
- Relative humidity (storage): max. 95% non-condensing
- Altitude: -300m to + 3,000m
- Shock: 15g/11ms
- Bump: 10g/16ms
- Vibration (sinusoidal): 2g/10..150Hz
- Conformal coating on request

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Technical Data

Safety
- PCB manufactured with a flammability rating of 94V-0 by UL recognized manufacturers

EMC
- Tested according to EN 55022 (radio disturbance), IEC1000-4-2 (ESD) and IEC1000-4-4 (burst)

BIOS
- MENMON™

Software Support
- VxWorks®
- MontaVista Linux, Professional Edition 3.1
- QNX®
- For more information on supported operating system versions and drivers see Software.

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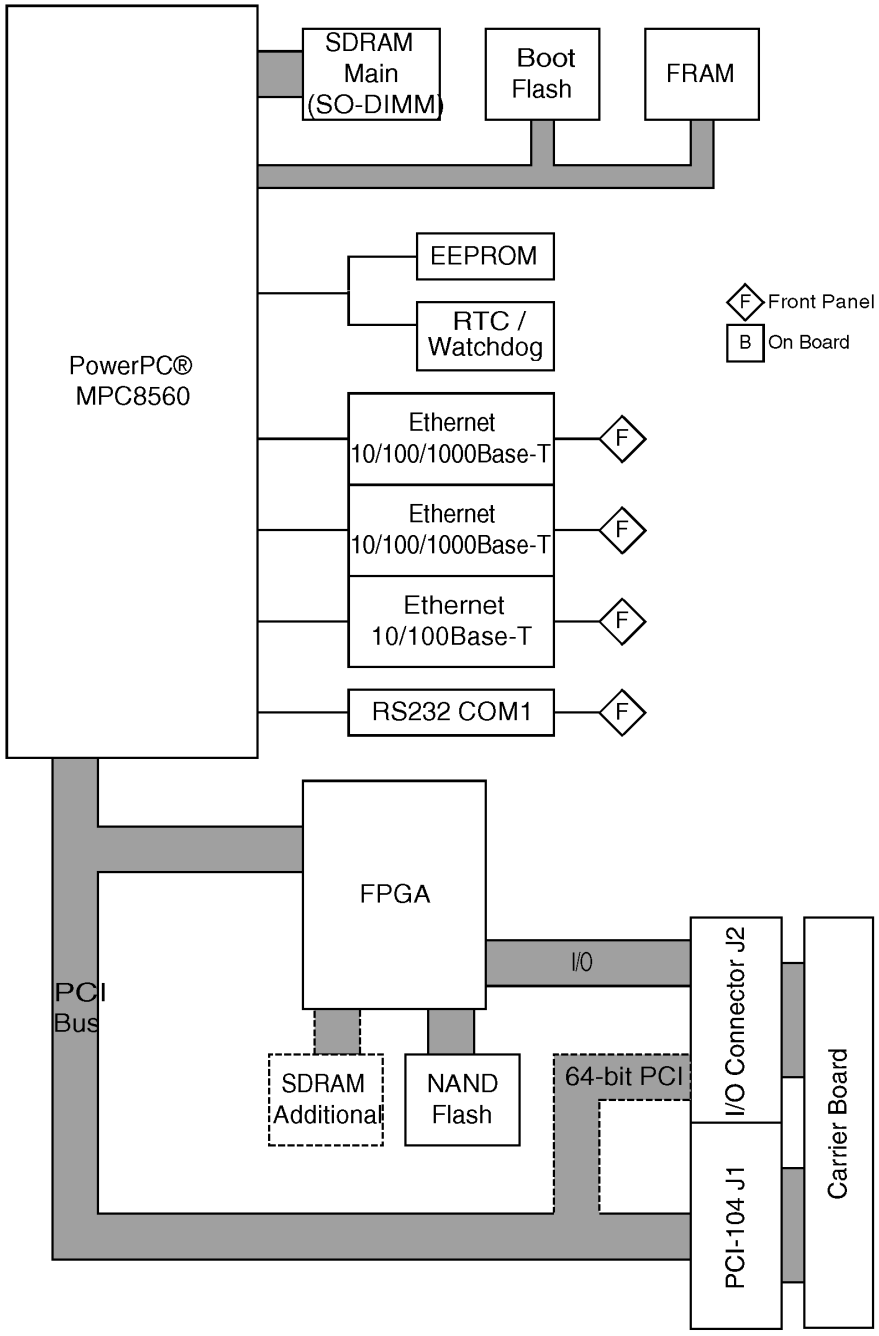
Diagram



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Configuration & Options

Standard Configurations

Article No.	CPU Type	Clock	System RAM	NAND Flash	Additional SDRAM	FRAM	Boot Flash	Operation Temperature
15EM03-00 (front I/O)	MPC8560	800 MHz	0 MB	128 MB	16 MB	32 KB	8 MB	0..+60°C
15EM03A00 (rear I/O)	MPC8560	800 MHz	0 MB	128 MB	16 MB	32 KB	8 MB	0..+60°C
15EM08-00 (front I/O)	MPC8540	800 MHz	0 MB	128 MB	16 MB	32 KB	8 MB	0..+60°C
15EM08A00 (rear I/O)	MPC8540	800 MHz	0 MB	128 MB	16 MB	32 KB	8 MB	0..+60°C

Options

Please note that some of these options may only be available for large volumes. Please ask our sales staff for more information.

CPU

- Type
  - MPC8540
  - MPC8560
- Clock
  - 666..833 MHz

Memory

- System RAM
  - 256 MB, 512 MB, 1 GB or 2 GB
  - With or without ECC
- NAND Flash
  - 0 MB up to maximum available
- Additional SDRAM
  - 0 MB or 16 MB
- FRAM
  - 0 MB or 32 MB
- Boot Flash
  - 8 MB or 16 MB

I/O

- Front Connections
  - D-Sub connectors for Ethernet and COM
  - LAN1 and LAN2 via one 9-pin D-Sub connector with 10/100Base-T support
  - LAN3 and COM1 via one 9-pin D-Sub connector (LAN3 always with 10/100Base-T)

Mechanical

- PCI and I/O connectors can also be placed for face-to-face assembly (ESM™ Type N)

Operation Temperature

- 0..+60°C

FPGA

Flexible Configuration

- This MEN board offers the possibility to add customized I/O functionality in FPGA.
- It depends on the board type, pin counts and number of logic elements which IP cores make sense and/or can be implemented. Please contact MEN for information on feasibility.
- You can find more information on our web page "User I/O in FPGA"

FPGA Capabilities

- FPGA Altera® Cyclone® EP1C12
  - 12,060 logic elements
  - 239,616 total RAM bits
- Connection
  - Available pin count: 47 pins
  - Functions available via I/O connector J2
- MEN offers a starter kit for a similar computer-on-module of the same product family. The kit includes a suitable carrier board with different I/O connectors for FPGA signals. An FPGA development package for this hardware kit is also available for download.

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Ordering Information

Standard Hardware

15EM03-00	MPC8560/800MHz, 128MB NAND Flash, 8MB boot Flash, 16MB graphics memory, 32KB FRAM, front: 2 Gigabit Ethernet (RJ45), 1 Fast Ethernet (RJ45), 1 UART (RJ45), 0..+60°C

Related Hardware

08EK07-00	ESM evaluation kit for EM8: Mini ATX carrier board, EM8 with PowerPC MPC8540/800MHz, 512MB SDRAM, 128MB NAND Flash, 32KB FRAM, 16MB graphics memory, 2 Gigabit Ethernet, 1 Fast Ethernet, 1 UART, graphics, IDE, RJ45 to D-Sub cable, VGA cable, external PSU and adapter for mounting of one PCI-104 module, 0..+60°C
15EM03A00	MPC8560/800MHz, 128MB NAND Flash, 8MB boot Flash, 16MB graphics memory, 32KB FRAM, 0..+60°C

Memory

0752-0174	256MB DDR RAM 0..+60°C for 15EM03-00 (no ECC)

Software: OS independent

13Z017-06	MDIS5 low-level driver sources (MEN) for 16Z034_GPIO and 16Z037_GPIO

Software: Linux

10EM03-90	MontaVista Linux LSP for EM3 and EM3A
13Z025-90	Linux native driver (MEN) for 16Z025_UART, 16Z057_UART and 16Z125_UART
13Z044-90	Linux native driver (MEN) for 16Z044_DISP (frame buffer)

Software: VxWorks

10EM03-60	VxWorks BSP (MEN) for EM3, EM3A, EM8, EM8A, EK7, A14C and F13
13Z025-60	VxWorks native driver (MEN) for 16Z025_UART, 16Z057_UART and 16Z125_UART

Software: QNX

10EM03-40	QNX BSP (MEN) for EM3, EM3A, EM8, EM8A, EK7, A14C and F13
13Z025-40	QNX native driver (MEN) for 16Z025_UART and 16Z125_UART
13Z044-40	QNX native driver (MEN) for 16Z044_DISP (frame buffer)

Software: Firmware/BIOS

14EM03-00	MENMON (Firmware) for EM3, EM3A, EM8, EM8A, A14C and F13 (object code)

Documentation

20EM00-00	ESM Specification
20EM03-00	EM3/EM3A/EM8/EM8A User Manual
20EM03-ER	EM3 Errata
21APPN009	Application Note: 16Z025_UART and 16Z125_UART under Linux
21MENM-00	MENMON 2nd Edition User Manual
22Z025-ER	16Z025_UART Errata

For the most up-to-date ordering information and direct links to other data sheets and downloads, see the EM3 online data sheet under » www.men.de.

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