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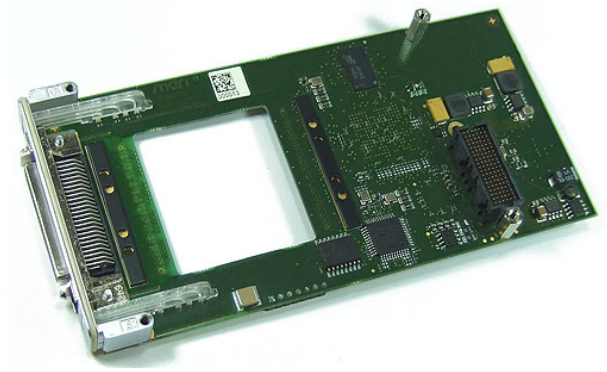
P699 - USM™ Main XMC



- **Main XMC for USM™ Universal Submodules**
- **PCIe® 2.5 Gbits/s**
- **1 USM™ slot**
- **1 FPGA 24,624 LE (for user-defined I/O)**
- **32 MB DDR2 SDRAM**
- **4 MB Flash**
- **-10 to +70°C screened**

USM™ Universal Submodules make XMC modules more flexible than ever. The main XMC P699 gets its specific function through the IP cores implemented inside the onboard FPGA. This function can be changed at any time through implementation of different IP cores. The corresponding line drivers are realized on the USM™ which is simply plugged on the P699.
The same USM™ may also be used on PMCs, conduction-cooled PMCs or M-Modules™ supporting the USM™ concept. A new design is then limited to the USM™ module and the FPGA content and therefore saves development time and costs. If local intelligence is needed, a Nios® soft processor can be implemented in the Cyclone® III FPGA on request.

The growing range of Wishbone-based standard IP cores from MEN comprise different UARTs, Ethernet, fieldbus interfaces, graphics, digital I/O etc.
The USM™ concept has been developed for harsh environments. Therefore, the P699 uses robust connectors to the USM™, while all other components are soldered, and operates in a -10 to +70 °C temperature range.
The P699 is an XMC mezzanine card suitable for any compliant host carrier board in any type of bus system, i.e. CPCI, VME or on any type of stand-alone SBC. Compared to PMC, the XMC standard defines a different board-to-board connector for support of PCI Express®. Appropriate carrier cards in 3U, 6U and other formats are available from MEN or other manufacturers.

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Technical Data

Functionality
- User-defined through FPGA
- Line drivers and/or additional hardware implemented on USM™ Universal Submodule (not included)

Memory
- 32MB SDRAM memory
  - Soldered
  - DDR2
  - 133MHz memory bus frequency
  - FPGA-controlled
- 4MB non-volatile Flash
  - For FPGA configuration data
  - FPGA-controlled
  - Serial SPI Flash, 33MHz

FPGA
- Standard factory FPGA configuration:
  - Chameleon Table V2
  - PCI Express® interface/PCIe® to Wishbone bridge
  - ID EEPROM emulation
  - 16Z069_RST - Reset controller
  - 16Z052_GIRQ - Interrupt controller
  - 16Z001_SMB - SMBus controller
  - 16Z126_SERFLASH - Serial Flash interface
  - 16Z043_SDRAM - DDR2 SDRAM controller
  - 16Z125_UART - UART controller
  - 16Z034_GPIO - GPIO controllers (3 IP cores, for onboard LEDs and 16-bit I/O)
- The FPGA offers the possibility to add customized I/O functionality. See FPGA.

USM™ Slot
- One slot for a standard USM™ module
- For implementation of line drivers and/or additional hardware

Miscellaneous
- Eight front-panel LEDs, FPGA-controlled
- I²C interface to detect the USM™ module

XMC Characteristics
- Compliant with XMC standard VITA 42.3-200x
- PCI Express® links: one x1

PCI Express®
- One x1 link
- Data rate 250MB/s in each direction (2.5 Gbits/s per lane)

Peripheral Connections
- Via front panel on a shielded 50-pin HP D-Sub SCSI 2 receptacle connector

Electrical Specifications
- Isolation voltage:
  - Voltage depends on implementation and signal routing of USM™
- Supply voltage/power consumption:
  - +5V and +12V (-5%/+5%)
  - +3.3V (-5%/+5%)
  - Consumption depends on FPGA and USM™ configuration

Mechanical Specifications
- Dimensions: conforming to IEEE 1386.1
- Weight: 70g (w/o USM™ module)

Environmental Specifications
- Temperature range (operation):
  - -10..+70°C (screened)
  - Airflow: min. 10m³/h
- Temperature range (storage): -40..+85°C
- Relative humidity (operation): max. 95% non-condensing
- Relative humidity (storage): max. 95% non-condensing
- Altitude: -300m to + 3,000m
- Shock: 15g/11ms
- Bump: 10g/16ms
- Vibration (sinusoidal): 2g/10..150Hz
- Conformal coating on request

MTBF
- 757,662h @ 40°C according to IEC/TR 62380 (RDF 2000)

Safety
- PCB manufactured with a flammability rating of 94V-0 by UL recognized manufacturers

EMC
- Conforming to EN 55022 (radio disturbance), IEC1000-4-2 (ESD) and IEC1000-4-4 (burst)

Software Support
- Flash update tools for Windows®, Linux, VxWorks®
- Driver software depending on implemented FPGA functions
- UART driver software for Windows® on request
- For more information on supported operating system versions and drivers see Software.

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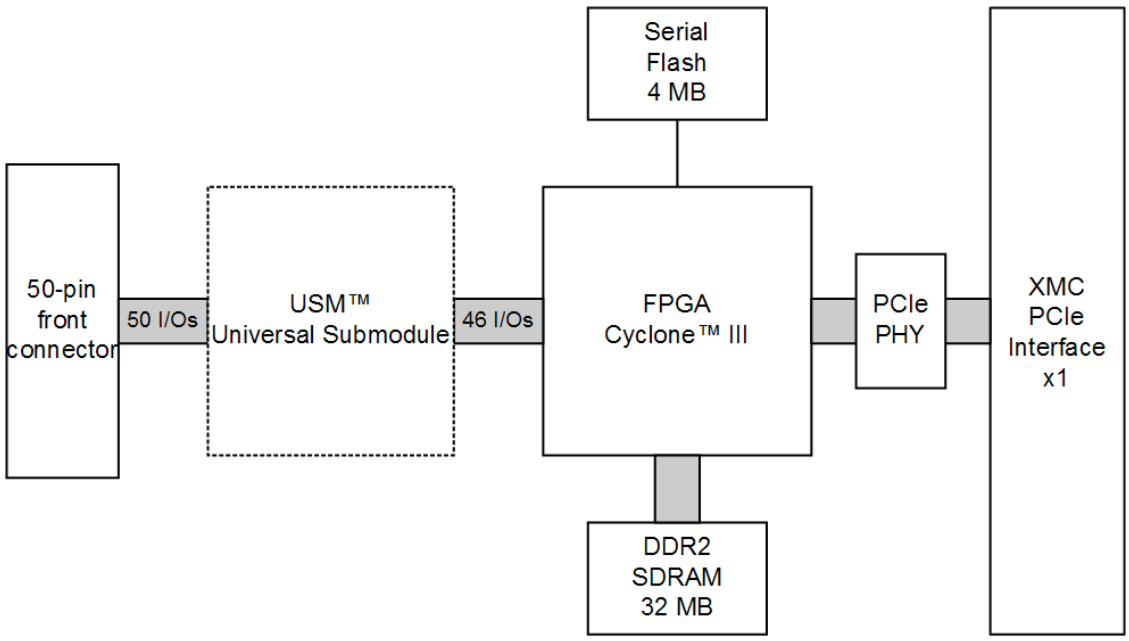
Diagram



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FPGA

Flexible Configuration

- This MEN board offers the possibility to add customized I/O functionality in FPGA.
- It depends on the board type, pin counts and number of logic elements which IP cores make sense and/or can be implemented. Please contact MEN for information on feasibility.
- You can find more information on our web page "User I/O in FPGA"

FPGA Capabilities

- FPGA Altera® Cyclone® III EP3C25
  - 24,624 logic elements
  - 594 Kbits total RAM
  - Supports Nios® II soft processor
- Connection
  - Functions can be linked to Wishbone bus
  - Available pin count: 46 pins (FPGA to USM™)
  - Functions available via USM™ at front I/O connector
- Functional updates via software
  - MEN offers Flash update tools for different operating systems.

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Ordering Information

Standard Hardware

15P699-00 USM main XMC, -10..+70°C screened

Related Hardware

19P599-00 PMC USM FPGA development kit consisting of 1 FPGA-based universal PMC P599, 1 bare USM Universal Submodule US0, 1 eval board AD99 for USM/FPGA development, 1 SA-Adapter SA1 (RS232), connection cable, FPGA/Nios example project including PCI core (key download), 0..+60°C

Miscellaneous

05P599-00 PMC/M-Module cable, 2m, with 50-pin HP D-Sub 50 M both sides, 0..+60°C

08US00-00 Universal Submodule for prototyping, -40..+85°C qualified

Software: OS independent

13Z017-06 MDIS5 low-level driver sources (MEN) for 16Z034_GPIO and 16Z037_GPIO

Software: Linux

13Z025-90 Linux native driver (MEN) for 16Z025_UART, 16Z057_UART and 16Z125_UART

13Z100-91 Linux FPGA update tool (MEN)

Software: Windows

13Z017-70 MDIS4/2004 / MDIS5 Windows driver (MEN) for 16Z034_GPIO devices

13Z100-70 Windows FPGA update tool (MEN)

Software: VxWorks

13Z025-60 VxWorks native driver (MEN) for 16Z025_UART, 16Z057_UART and 16Z125_UART

13Z100-60 VxWorks FPGA update tool (MEN)

Software: QNX

13Z100-40 QNX FPGA update tool (MEN)

Documentation

20P699-00 P699 User Manual

20US00-00 USM Specification

21M199-00 P599/M199 Programmer's Guide

For the most up-to-date ordering information and direct links to other data sheets and downloads, see the P699 online data sheet under » www.men.de.

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