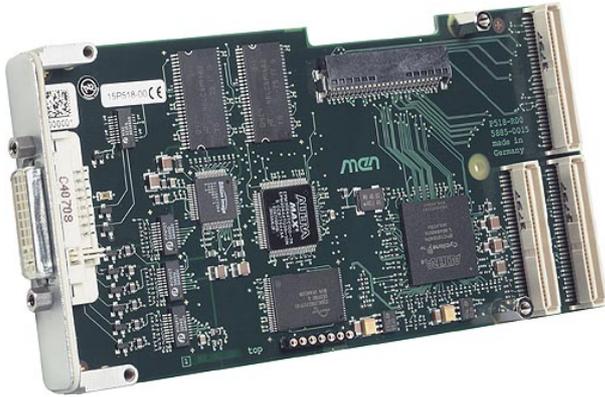


P518 - Frame Buffer Interface PMC



- **Frame buffer functionality in FPGA**
- **FPGA 12,000 LEs (approx.144,000 gates)**
- **Color depth 16-bit RGB**
- **640 x 480 up to 1280 x 1024 pixels resolution**
- **Frequencies 60 Hz and 75 Hz**
- **32 MB integrated graphics RAM**
- **DVI digital video output (DVI-I front connector)**
- **LVDS TFT via rear-I/O or on-board connector**
- **-40 to +85°C with qualified components**

The P518 comes with frame buffer functionality and is typically used as an extension card for PCI-based systems. The complete set of graphics instructions is realized inside an FPGA, with the FPGA acting as a PCI target (32-bit/33-MHz or 32-bit/66-MHz). Using FPGA technology to implement graphics in a system provides the advantage of nearly unlimited availability - which is ideal for industrial applications. And since the FPGA is available in -40 to +85°C operation temperature from the chip manufacturer, the complete P518 module is delivered in this extended temperature range.

The P518 is equipped with a DVI digital video output connector. An LVDS TFT interface is accessible via the on-board connector or the rear-I/O connector. A 32-MB, 133-MHz SDRAM is implemented as a local frame buffer. Its data bus width is 32 bits.

Multiple display modes are configurable by updating a configuration Flash. The graphics controller itself will be loaded with the new Flash data via a small configuration PLD after restart.

The graphics controller video outputs are flat panel signals. Conversion to both VGA and DVI is done by separate hardware.

The graphics clock is supplied directly by a 48-MHz oscillator.

The same functionality is also available on PC-MIP®, a PCI-based mezzanine card in a smaller form factor.

The P518 is a PMC mezzanine card suitable for any PMC compliant host carrier board in any type of bus system, i.e. CPCI, VME or on any type of stand-alone SBC. Appropriate PMC carrier cards in 3U, 6U and other formats are available from MEN or other manufacturers.

Technical Data

Video Signals

- DVI interface; FP to DVI conversion
- VGA interface; FP to VGA conversion
- LVDS TFT interface via rear I/O
- Color depth 16-bit RGB
- Resolutions DVI/VGA (change only by FPGA update)
 - 640 x 480
 - 800 x 600
 - 1024 x 768
 - 1280 x 1024
- Resolutions LVDS (change only by FPGA update)
 - 640 x 480, 800 x 600 or 1024 x 768 with one or two LVDS connections
 - 1280 x 1024 with two LVDS connections only
- Frequencies: DVI/VGA 60Hz or 75Hz; LVDS 60Hz

Memory

- 32MB/133MHz SDRAM with 32-bit memory interface

FPGA

- Standard FPGA graphics configuration
 - Main bus interface
 - 16Z044_DISP - Display controller
 - 16Z043_SDRAM - SDRAM controller
 - 16Z045_FLASH - Flash interface
- The FPGA offers the possibility to add customized I/O functionality. See FPGA.
- Examples of graphics extensions:
 - Video compression
 - Bit blitter
 - Rendering
 - Pattern recognition
 - ...

Peripheral Connection

- Flat-panel and VGA signals via DVI-I front connector
- LVDS signals via Pn4 rear I/O or P1 onboard connector

PMC Characteristics (PCI)

- Compliant with PCI Specification 2.2
- 32-bit/33-MHz, 3.3V V(I/O); 66MHz on request
- Target

Electrical Specifications

- Supply voltage/power consumption:
 - +5V (4.85V..5.25V), 10mA max.
 - +3.3V (3.0V..3.6V), 300mA typ.

Mechanical Specifications

- Dimensions: conforming to IEEE 1386.1
- Weight: 70g

Environmental Specifications

- Temperature range (operation):
 - -40..+85°C
 - Airflow: min. 10m³/h
- Temperature range (storage): -40..+85°C
- Relative humidity (operation): max. 95% non-condensing
- Relative humidity (storage): max. 95% non-condensing
- Altitude: -300m to + 3,000m
- Shock: 15g/11ms
- Bump: 10g/16ms
- Vibration (sinusoidal): 2g/10..150Hz
- Conformal coating on request

MTBF

- MTBF: 426,000h @ 40°C (derived from MIL-HDBK-217F)

Safety

- PCB manufactured with a flammability rating of 94V-0 by UL recognized manufacturers

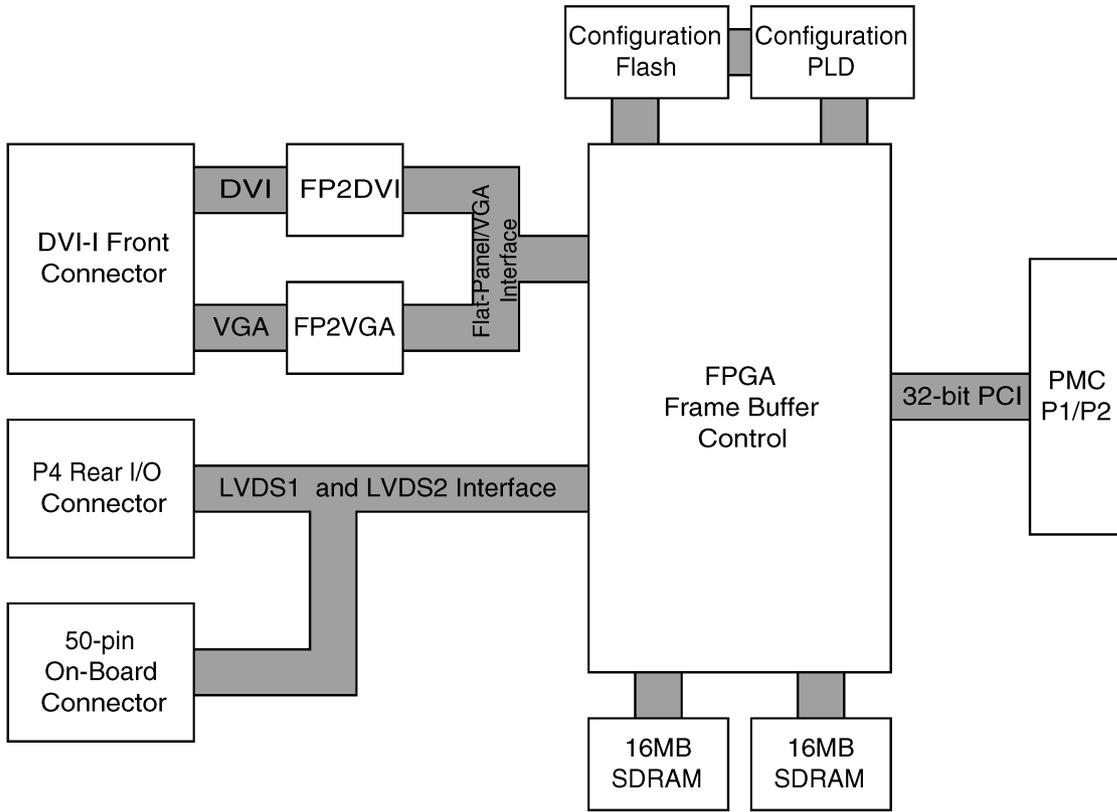
EMC

- Tested according to EN 55022 (radio disturbance), IEC1000-4-2 (ESD) and IEC1000-4-4 (burst)

Software Support

- Windows®
- Linux
- VxWorks® (WindML)
- For more information on supported operating system versions and drivers see Software.

Diagram



Configuration & Options

Standard Configurations

Article No.	Resolution	SGRAM	Operation Temperature
15P518-00	800 x 600	32 MB	-40..+85°C

Options

Resolution

- 640 x 480
- 800 x 600
- 1024 x 768
- 1280 x 1024 (two LVDS connections needed for LVDS support!)

SGRAM

- 16 MB or 32 MB

Operation Temperature

- -40..+85°C

Please note that some of these options may only be available for large volumes. Please ask our sales staff for more information.

FPGA

Flexible Configuration

- This MEN board offers the possibility to add customized I/O functionality in FPGA.
- It depends on the board type, pin counts and number of logic elements which IP cores make sense and/or can be implemented. Please contact MEN for information on feasibility.
- [You can find more information on our web page "User I/O in FPGA"](#)

FPGA Capabilities

- FPGA Altera® Cyclone® EP1C12
 - 12,060 logic elements
 - 239,616 total RAM bits
- Configuration data stored in 2MB Flash
- MEN offers Flash update tools for different operating systems.

Ordering Information

Standard Hardware

15P518-02 FPGA-based frame buffer interface, resolution 800x600, 32MB integrated SGRAM, without rear I/O, -40..+85°C with qualified components

Miscellaneous

05F007-02 DVI-to-VGA cable, DVI plug to 15-pin HD-Sub plug, 2m, -20..+70°C

05F007-03 Adapter, DVI analog plug to VGA 15-pin HD-Sub receptacle, -20..+70°C

FPGA Packages

16P018-00 P518/P18 FPGA file for frame buffer functionality (PCI, SDRAM, 18-bit TTL RGB, LVDS, Flash)

Software: Linux

13Z044-90 Linux native driver (MEN) for 16Z044_DISP (frame buffer)

13Z100-91 Linux FPGA update tool (MEN)

Software: Windows

13Z044-70 Windows native driver (MEN) for 16Z044_DISP (frame buffer)

13Z100-70 Windows FPGA update tool (MEN)

Software: VxWorks

13Z044-60 VxWorks driver (MEN) for 16Z044_DISP (frame buffer)

13Z100-60 VxWorks FPGA update tool (MEN)

Software: QNX

13Z044-40 QNX native driver (MEN) for 16Z044_DISP (frame buffer)

13Z100-40 QNX FPGA update tool (MEN)

Software: FPGA

16P018-00 P518/P18 FPGA file for frame buffer functionality (PCI, SDRAM, 18-bit TTL RGB, LVDS, Flash)

Documentation

20P518-00 P518 User Manual

For the most up-to-date ordering information and direct links to other data sheets and downloads, see the P518 online data sheet under » www.men.de.

Contact Information

Germany

MEN Mikro Elektronik GmbH
 Neuwieder Straße 5-7
 90411 Nuremberg
 Phone +49-911-99 33 5-0
 Fax +49-911-99 33 5-901
 E-mail info@men.de
 www.men.de

France

MEN Mikro Elektronik SA
 18, rue René Cassin
 ZA de la Châtelaine
 74240 Gaillard
 Phone +33 (0) 450-955-312
 Fax +33 (0) 450-955-211
 E-mail info@men-france.fr
 www.men-france.fr

USA

MEN Micro, Inc.
 24 North Main Street
 Ambler, PA 19002
 Phone (215) 542-9575
 Fax (215) 542-9577
 E-mail sales@menmicro.com
 www.menmicro.com

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