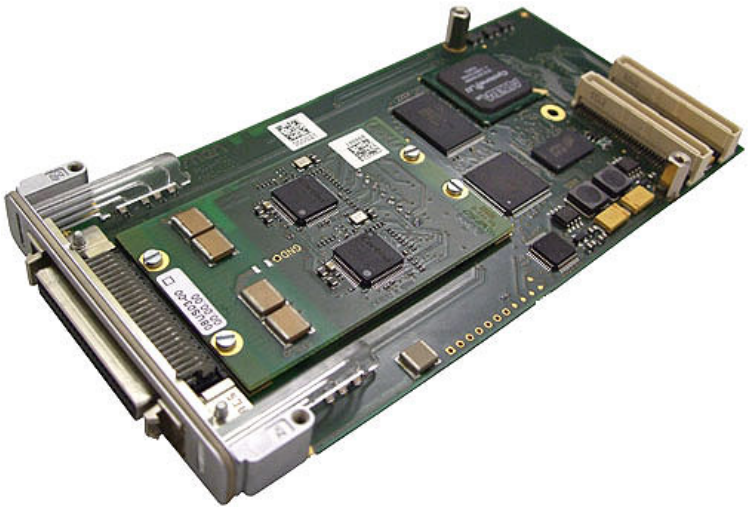
P511 – Dual Fast Ethernet PMC

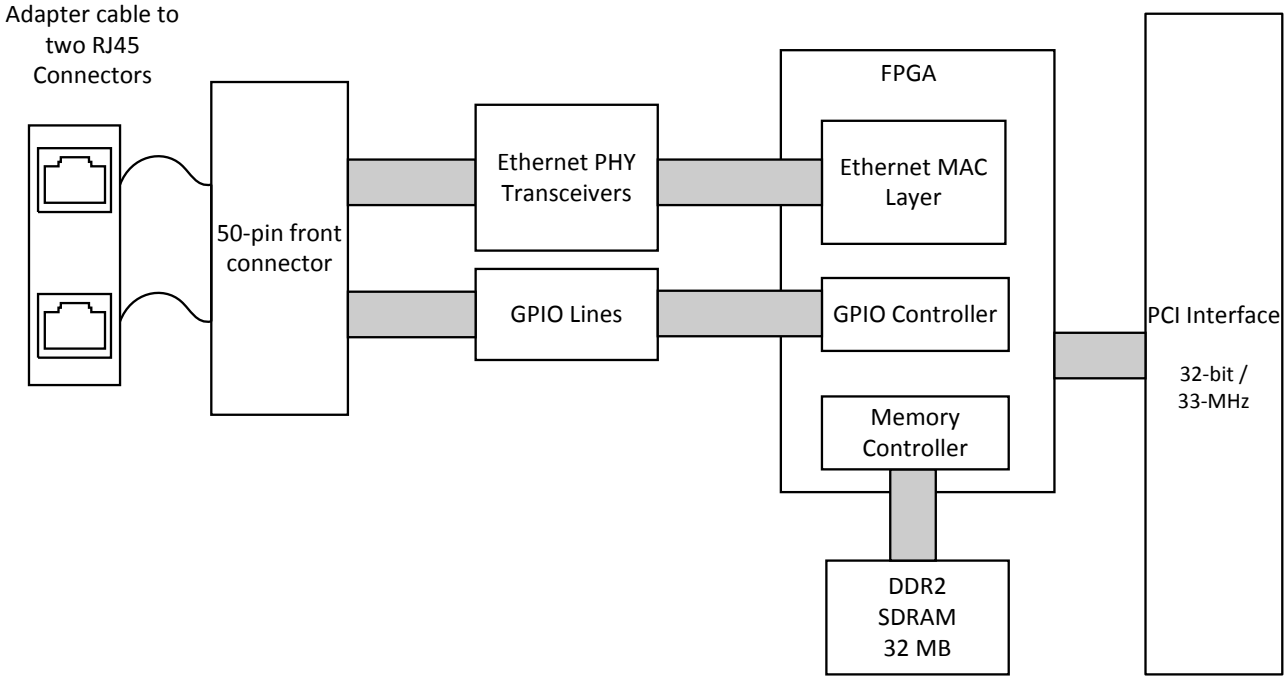
- **2 full-duplex or half-duplex channels**
- **10Base-T and 100Base-TX physical layer**
- **MAC layer realized in FPGA**
- **Local or external data buffer**
- **6 additional GPIOs**
- **Fully integrated to comply with IEEE802.3**
- **1500 VAC isolation voltage**
- **-40 to +85°C with qualified components**
- **32-bit/33-MHz PMC**
- **PMC based on USM concept**
- **Individual FPGA configuration**



The P511 is a 32bit/33MHz PMC with dual Ethernet functionality. The two channels can be accessed via two RJ45 connectors which are led to the front via an adapter cable from a SCSI connector. They support half duplex and full duplex operation.
The PMC offers the possibility to buffer all receive and transmit Ethernet frames either in a local or in an external data buffer. This makes it possible to provide a Worst Case Execution Time analysis which makes it particularly well suited for safety-critical applications.
Up to 6 GPIO lines can be used on the module for additional functionality.

The P511 is based on the USM concept. USM Universal Submodules make PMC modules more flexible than ever. The Ethernet functionality is realized via an IP core implemented inside its onboard FPGA. This function can be changed at any time through implementation of different IP cores. The corresponding line drivers are realized on the USM which is simply plugged on the P511. One alternative function is the combination of an Ethernet core with a fieldbus interface to build gateways.
The I/O mezzanine module is suitable for any PMC compliant host carrier board in any type of bus system, i.e. CPCI, VME or on any type of stand-alone SBC in telecommunication, industrial, medical, transportation or aerospace applications. It offers long-term availability for at least 10 years and is qualified for operation in the extended temperature range.

Diagram


Adapter cable to two RJ45 Connectors
50-pin front connector
Ethernet PHY Transceivers
GPIO Lines
FPGA
Ethernet MAC Layer
GPIO Controller
Memory Controller
DDR2 SDRAM 32 MB
PCI Interface
32-bit / 33-MHz

Technical Data

Ethernet Interface	■ Two 10/100Base-T Ethernet channels ■ Accessible on two RJ45 connectors via adapter cable ■ Half duplex/full duplex support
Memory	■ 32MB SDRAM memory □ Soldered □ DDR2 □ 132MHz memory bus frequency □ FPGA-controlled ■ 2MB non-volatile Flash □ For FPGA data and Nios® firmware □ FPGA-controlled
GPIO	■ Up to six lines controlled via software
FPGA	■ Standard factory FPGA configuration: □ Main bus interface □ Interrupt controller, SMBus controller □ 16Z087_ETH - Ethernet MAC IP core (2 IP cores for the 2 channels) □ 16Z043_SDRAM - SDRAM controller □ 16Z045_FLASH - Flash interface □ 16Z034_GPIO - GPIO controllers (2 IP cores, for onboard LEDs and 8-bit I/O) ■ The FPGA offers the possibility to add customized I/O functionality. See FPGA.
PMC Characteristics (PCI)	■ Compliant with PCI Specification 2.2 ■ 32-bit/33-MHz, 3.3V V(I/O) ■ Target and initiator
Peripheral Connections	■ Via front panel on a shielded 50-pin HP D-Sub SCSI 2 receptacle connector ■ Adapter cable to two RJ45 connectors included in the delivery
Electrical Specifications	■ Isolation voltage: □ 1500 VAC ■ Supply voltage/power consumption: □ +5V (-3%/+5%), 40mA □ +3.3V (-5%/+5%), 139mA
Mechanical Specifications	■ Dimensions: conforming to IEEE 1386.1 ■ Weight: 78g
Environmental Specifications	■ Temperature range (operation): □ -40..+85°C (qualified components) □ Airflow: min. 1.0m/s ■ Temperature range (storage): -40..+85°C ■ Relative humidity (operation): max. 95% non-condensing ■ Relative humidity (storage): max. 95% non-condensing ■ Altitude: -300m to + 3,000m ■ Shock: 15g/11ms ■ Bump: 10g/16ms ■ Vibration (sinusoidal): 1g/10..150Hz ■ Conformal coating on request
MTBF	■ 1 305 649 h @ 40°C according to IEC/TR 62380 (RDF 2000)
Safety	■ PCB manufactured with a flammability rating of 94V-0 by UL recognized manufacturers
EMC	■ Conforming to EN 55022 (radio disturbance), IEC1000-4-2 (ESD) and IEC1000-4-4 (burst)

Technical Data

Software Support	■ Windows® ■ Linux ■ QNX® ■ For more information on supported operating system versions and drivers see Downloads.

FPGA

This product offers the possibility to add customized I/O functionality in FPGA.

Flexible Configuration	■ Customized I/O functions can be added to the FPGA. ■ It depends on the board type, pin counts and number of logic elements which IP cores make sense and/or can be implemented. Please contact MEN for information on feasibility. ■ You can find more information on our web page "User I/O in FPGA"
FPGA Capabilities	■ FPGA Altera® Cyclone® II EP2C35 □ 33,216 logic elements □ 483,840 total RAM bits □ Supports Nios® II soft processor ■ Connection □ Functions can be linked to Wishbone or Avalon® bus □ Available pin count: 46 pins (FPGA to USM) □ Functions available via USM at front I/O connector ■ MEN offers a USM development kit and an FPGA Development Package as well as Flash update tools for different operating systems.

Configuration & Options

Standard Configurations

Article No.	Main FPGA Content	Soft Core	Memory	Signals	Cooling Method	Operation Temperature
15P511-00	2 Fast Ethernet Cores	No	32 MB RAM, 2 MB Flash	Front	Convection	-40..+85°C

Options

CPU	■ Nios® soft core implementation possible (e.g. for real-time Ethernet)
Rear I/O	■ Via Pn4 rear I/O connector
Cooling	■ Conduction Cooling

Please note that some of these options may only be available for large volumes. Please ask our sales staff for more information.

Ordering Information

Standard P511 Models	**15P511-00**	Dual Fast Ethernet, 2 Ethernet cores, 6 GPIO signals, front I/O, for convection cooled systems, -40..+85°C with qualified components
Miscellaneous Accessories	**05P000-01**	25 mounting screw sets to fix PMC/XMC modules on carrier boards
	05P511-00	P511 Ethernet HDSUB to 2 x RJ45 cable, -40..+85°C
Software: Linux	This product is designed to work under Linux. See below for potentially available separate software packages from MEN.	
	13Z001-90	Linux host driver (MEN) for 16Z001_SMB (I2C)
	13Z077-90	Linux native driver (MEN) for 16Z077_ETH and 16Z087_ETH
Software: Windows®	This product is designed to work under Windows®. See below for potentially available separate software packages from MEN.	
	10Y000-78	Windows® Embedded Standard 7 BSP for F11S, F19P, F21P, F22P, G20, G22, XM1L, XM2, MM1, MM2, SC21, SC24, SC27, BC50M, BC50I, BL50W, BL50S, DC13, F206, F210, F215, F216, G215, P506, P507 and P511
	13P511-77	Windows® Installset (MEN) for P511 (Includes all free drivers developed by MEN for the supported hardware.)
	13Z087-70	Windows® native driver (MEN) for 16Z087_ETH (Ethernet controller)
Software: QNX®	This product is designed to work under QNX®. For details regarding supported/unsupported board functions please refer to the corresponding software data sheets.	
	13Z087-40	QNX® native driver (MEN) for 16Z087_ETH

For operating systems not mentioned here contact MEN sales.

Documentation	Compare Chart mezzanine functions on PMC/XMC and PC-MIP® » Download	
	20P511-00	P511 User Manual
	22Z087-ER	16Z087_ETH Errata

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