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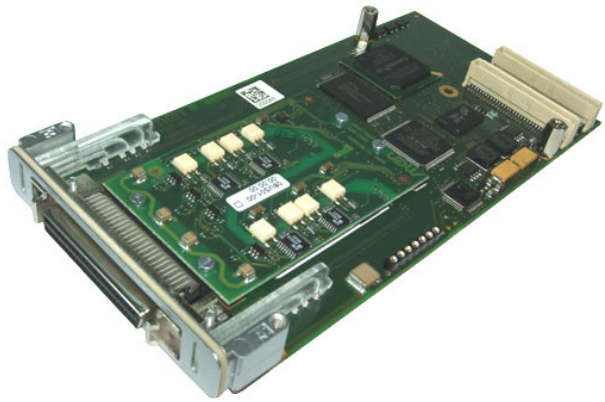
P507 - Quad RS422/485 Interface PMC



- **32-bit/33-MHz PMC**
- **4 high-performance UARTs**
- **Full and half duplex, software programmable**
- **Serial data rates up to 921,600 bits/s**
- **Isolation between channels**
- **-40 to +85°C with qualified components**

The P507 is a high-performance quadruple UART with RS422/485 interface. It supports full duplex (with RS422) and half duplex operation (with RS485) and data rates of up to 921,600 bit/s. Each channel has its own 500V isolation, with all ports being available on the 50-pin D-Sub front connector.
The P507 is based on the USM™ concept. USM™ Universal Submodules make PMC modules more flexible than ever. The UART interfaces are realized via four IP cores implemented inside its onboard FPGA. This function can be changed at any time through implementation of different IP cores. The corresponding line drivers are realized on the USM™ which is simply plugged on the P507.
The module is suitable for any PMC compliant host carrier board in any type of bus system, i.e. CPCI, VME or on any type of stand-alone SBC in telecommunication, industrial, medical, transportation or aerospace applications. It offers long-term availability for at least 10 years and is qualified for operation in the extended temperature range.

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Technical Data

UART Interfaces
- Four RS422/RS485 UARTs
- Software-configurable
- Data rates up to 921,600 bits/s
- 60-byte transmit/receive buffer
- Full-duplex operation with RS422, half-duplex operation with RS485
- Isolation between channels: 500V
- Compatible with 16550 UART

Memory
- 32MB SDRAM memory
  - Soldered
  - DDR2
  - 132MHz memory bus frequency
  - FPGA-controlled
- 2MB non-volatile Flash
  - For FPGA data and Nios® firmware
  - FPGA-controlled

FPGA
- Standard factory FPGA configuration:
  - Main bus interface
  - Interrupt controller, SMBus controller
  - 16Z125_UART - UART Controller
  - 16Z043_SDRAM - SDRAM controller
  - 16Z045_FLASH - Flash interface
  - 16Z034_GPIO - GPIO controller
- The FPGA offers the possibility to add customized I/O functionality. See FPGA.

PMC Characteristics (PCI)
- Compliant with PCI Specification 2.2
- 32-bit/33-MHz, 3.3V V(I/O)
- Target

Peripheral Connections
- Via front panel on a shielded 50-pin HP D-Sub SCSI 2 receptacle connector

Electrical Specifications
- Isolation voltage:
  - 500 VAC
- Supply voltage/power consumption:
  - +5V (-3%/+5%), 120mA
  - +3.3V (-5%/+5%), 9mA

Mechanical Specifications
- Dimensions: conforming to IEEE 1386.1
- Weight: 78g

Environmental Specifications
- Temperature range (operation):
  - -40..+85°C (qualified components)
  - Airflow: min. 1.0m/s
- Temperature range (storage): -40..+85°C
- Relative humidity (operation): max. 95% non-condensing
- Relative humidity (storage): max. 95% non-condensing
- Altitude: -300m to + 3,000m
- Shock: 15g/11ms
- Bump: 10g/16ms
- Vibration (sinusoidal): 1g/10..150Hz
- Conformal coating on request

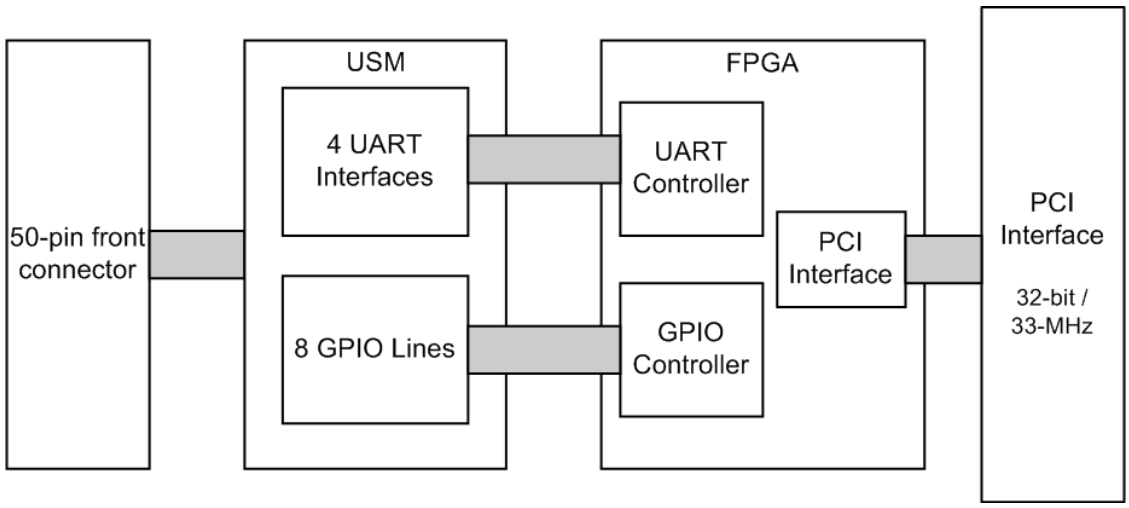
MTBF
- tbd @ 40°C according to IEC/TR 62380 (RDF 2000)

Safety
- PCB manufactured with a flammability rating of 94V-0 by UL recognized manufacturers

EMC
- Conforming to EN 55022 (radio disturbance), IEC1000-4-2 (ESD) and IEC1000-4-4 (burst)

Software Support
- Windows®
- Linux
- For more information on supported operating system versions and drivers see Software.

Diagram


50-pin front connector
USM
4 UART Interfaces
8 GPIO Lines
FPGA
UART Controller
GPIO Controller
PCI Interface
PCI Interface
32-bit / 33-MHz

Configuration & Options

Standard Configurations

Article No.	Main FPGA Content	Soft Core	Memory	Signals	Cooling Method	Operation Temperature
15P507-00	4 RS422/485 interfaces	No	32 MB RAM, 2 MB Flash	Front	Convection	-40..+85°C

Options

CPU

- Nios® soft core implementation possible (e.g. for real-time Ethernet)

Rear I/O

- Via Pn4 rear I/O connector

Cooling

- Conduction Cooling

Please note that some of these options may only be available for large volumes. Please ask our sales staff for more information.

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FPGA

Flexible Configuration

- This MEN board offers the possibility to add customized I/O functionality in FPGA.
- It depends on the board type, pin counts and number of logic elements which IP cores make sense and/or can be implemented. Please contact MEN for information on feasibility.
- You can find more information on our web page "User I/O in FPGA"

FPGA Capabilities

- FPGA Altera® Cyclone® II EP2C35
  - 33,216 logic elements
  - 483,840 total RAM bits
  - Supports Nios® II soft processor
- Connection
  - Functions can be linked to Wishbone or Avalon® bus
  - Available pin count: 46 pins (FPGA to USM™)
  - Functions available via USM™ at front I/O connector
- MEN offers a USM™ development kit and an FPGA Development Package as well as Flash update tools for different operating systems.

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Ordering Information

Standard Hardware

15P507-00 Quad RS422/485 interface, 4 UART cores, front I/O, for convection cooled systems, -40..+85°C with qualified components

Software: OS independent

13Z017-06 MDIS5 low-level driver sources (MEN) for 16Z034_GPIO and 16Z037_GPIO

Software: Linux

13Z025-90 Linux native driver (MEN) for 16Z025_UART, 16Z057_UART and 16Z125_UART

Software: Windows

13P507-77 WindowsInstallset (MEN) for P507

Documentation

20P507-00 P507 User Manual

For the most up-to-date ordering information and direct links to other data sheets and downloads, see the P507 online data sheet under » www.men.de.

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