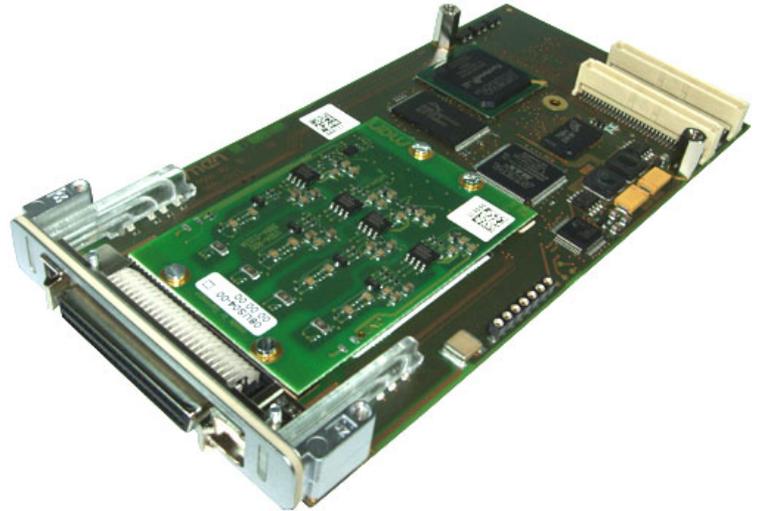


# P506 – Quad CAN Bus Interface PMC

- **32-bit/33-MHz PMC**
- **Full CAN/Extended CAN**
- **4 independent channels**
- **ISO high-speed coupling**
- **Up to 1 Mbit/s data transfer rate**
- **CANopen master and slave support**
- **CAN Layer 2 support**
- **Isolation between channels**
- **Compliant to ISO 11898-1 and ISO 11898-2**
- **-40 to +85°C with qualified components**



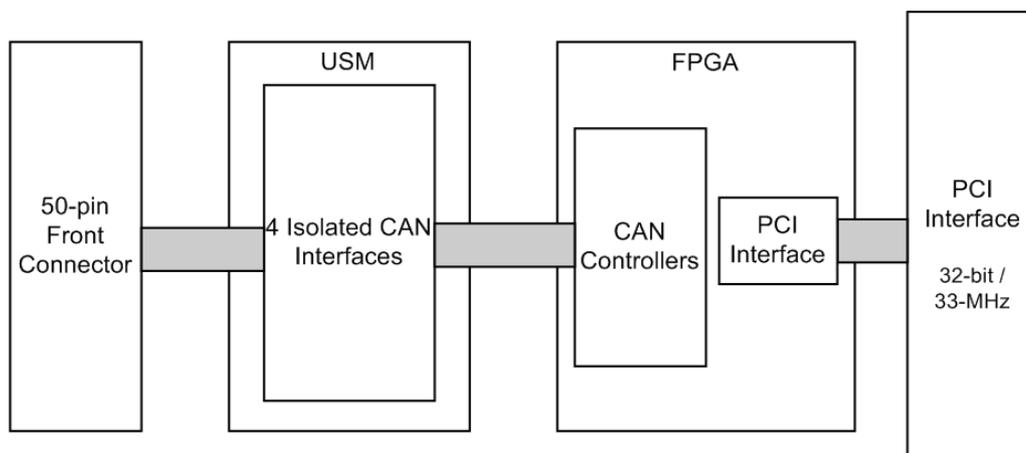
The P506 is a 32-bit/33MHz PMC with four CAN interfaces. They support CAN Protocol Version 2.0A/B, standard and extended data frames, remote frames, 0..8 bytes data length and a programmable data rate of up to 1 Mbit/s.

The P506 is based on the USM concept. USM Universal Submodules make PMC modules more flexible than ever. The CAN bus interfaces are realized via four IP cores implemented inside its onboard FPGA. This

function can be changed at any time through implementation of different IP cores. The corresponding line drivers are realized on the USM which is simply plugged on the P506.

The I/O mezzanine module is suitable for any PMC compliant host carrier board in any type of bus system, i.e. CPCI, VME or on any type of stand-alone SBC in telecommunication, industrial, medical, transportation or aerospace applications. It offers long-term availability for at least 10 years and is qualified for operation in the extended temperature range.

## Diagram



## Technical Data

<b>CAN Interface</b>	<ul style="list-style-type: none"> <li>■ Compliant to ISO 11898-1 and ISO 11898-2</li> <li>■ Four channels</li> <li>■ CAN Protocol Version 2.0A/B             <ul style="list-style-type: none"> <li>□ Standard and extended data frames</li> <li>□ 0..8 bytes data length</li> <li>□ Programmable data rate up to 1 Mbit/s</li> </ul> </li> <li>■ Support for remote frames</li> <li>■ 5 receive buffers (FIFO-scheme)</li> <li>■ 3 transmit buffers with prioritization</li> <li>■ Maskable identifier filter</li> <li>■ Programmable loop-back mode for self-test operation</li> <li>■ Signaling and interrupt capabilities for receiver and transmitter error states</li> </ul>
<b>Memory</b>	<ul style="list-style-type: none"> <li>■ 32MB SDRAM memory             <ul style="list-style-type: none"> <li>□ Soldered</li> <li>□ DDR2</li> <li>□ 132MHz memory bus frequency</li> <li>□ FPGA-controlled</li> </ul> </li> <li>■ 2MB non-volatile Flash             <ul style="list-style-type: none"> <li>□ For FPGA data and Nios® firmware</li> <li>□ FPGA-controlled</li> </ul> </li> </ul>
<b>FPGA</b>	<ul style="list-style-type: none"> <li>■ Standard factory FPGA configuration:             <ul style="list-style-type: none"> <li>□ Main bus interface</li> <li>□ Interrupt controller, SMBus controller</li> <li>□ <a href="#">16Z029_CAN - CAN Controller</a></li> <li>□ <a href="#">16Z043_SDRAM - SDRAM controller</a></li> <li>□ <a href="#">16Z045_FLASH - Flash interface</a></li> <li>□ <a href="#">16Z034_GPIO - GPIO controller</a></li> <li>□ <a href="#">16Z034_PWM - PWM Pulse Width Modulation</a></li> </ul> </li> <li>■ The FPGA offers the possibility to add customized I/O functionality. See FPGA.</li> </ul>
<b>PMC Characteristics (PCI)</b>	<ul style="list-style-type: none"> <li>■ Compliant with PCI Specification 2.2</li> <li>■ 32-bit/33-MHz, 3.3V V(I/O)</li> <li>■ Target</li> </ul>
<b>Peripheral Connections</b>	<ul style="list-style-type: none"> <li>■ Via front panel on a shielded 50-pin HP D-Sub SCSI 2 receptacle connector</li> </ul>
<b>Electrical Specifications</b>	<ul style="list-style-type: none"> <li>■ Isolation voltage:             <ul style="list-style-type: none"> <li>□ 500 VAC</li> </ul> </li> <li>■ Supply voltage/power consumption:             <ul style="list-style-type: none"> <li>□ +5V (-3%/+5%), 240mA</li> <li>□ +3.3V (-5%/+5%), 15mA</li> </ul> </li> </ul>
<b>Mechanical Specifications</b>	<ul style="list-style-type: none"> <li>■ Dimensions: conforming to IEEE 1386.1</li> <li>■ Weight: 78g</li> </ul>
<b>Environmental Specifications</b>	<ul style="list-style-type: none"> <li>■ Temperature range (operation):             <ul style="list-style-type: none"> <li>□ -40..+85°C (qualified components)</li> <li>□ Airflow: min. 1.0m/s</li> </ul> </li> <li>■ Temperature range (storage): -40..+85°C</li> <li>■ Relative humidity (operation): max. 95% non-condensing</li> <li>■ Relative humidity (storage): max. 95% non-condensing</li> <li>■ Altitude: -300m to + 3,000m</li> <li>■ Shock: 15g/11ms</li> <li>■ Bump: 10g/16ms</li> <li>■ Vibration (sinusoidal): 1g/10..150Hz</li> <li>■ Conformal coating on request</li> </ul>
<b>MTBF</b>	<ul style="list-style-type: none"> <li>■ 957 834 h @ 40°C according to IEC/TR 62380 (RDF 2000)</li> </ul>

## Technical Data

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<b>Safety</b>	<ul style="list-style-type: none"><li>■ PCB manufactured with a flammability rating of 94V-0 by UL recognized manufacturers</li></ul>
<b>EMC</b>	<ul style="list-style-type: none"><li>■ Conforming to EN 55022 (radio disturbance), IEC1000-4-2 (ESD) and IEC1000-4-4 (burst)</li></ul>
<b>Software Support</b>	<ul style="list-style-type: none"><li>■ Windows®</li><li>■ Linux</li><li>■ VxWorks®</li><li>■ QNX®</li><li>■ <a href="#">For more information on supported operating system versions and drivers see Downloads.</a></li></ul>

## FPGA

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This product offers the possibility to add customized I/O functionality in FPGA.

<b>Flexible Configuration</b>	<ul style="list-style-type: none"><li>■ Customized I/O functions can be added to the FPGA.</li><li>■ It depends on the board type, pin counts and number of logic elements which IP cores make sense and/or can be implemented. Please contact MEN for information on feasibility.</li><li>■ <a href="#">You can find more information on our web page "User I/O in FPGA"</a></li></ul>
<b>FPGA Capabilities</b>	<ul style="list-style-type: none"><li>■ FPGA Altera® Cyclone® II EP2C35<ul style="list-style-type: none"><li>□ 33,216 logic elements</li><li>□ 483,840 total RAM bits</li><li>□ Supports Nios® II soft processor</li></ul></li><li>■ Connection<ul style="list-style-type: none"><li>□ Functions can be linked to Wishbone or Avalon® bus</li><li>□ Available pin count: 46 pins (FPGA to USM)</li><li>□ Functions available via USM at front I/O connector</li></ul></li><li>■ <a href="#">MEN offers a USM development kit and an FPGA Development Package as well as Flash update tools for different operating systems.</a></li></ul>

## Configuration & Options

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### Standard Configurations

Article No.	Main FPGA Content	Soft Core	Memory	Signals	Cooling Method	Operation Temperature
15P506-00	4 CAN bus interfaces	No	32 MB RAM, 2 MB Flash	Front	Convection	-40..+85°C

### Options

<b>CPU</b>	■ Nios® soft core implementation possible (e.g. for real-time Ethernet)
<b>Rear I/O</b>	■ Via Pn4 rear I/O connector
<b>Cooling</b>	■ Conduction Cooling

Please note that some of these options may only be available for large volumes. Please ask our sales staff for more information.

## Ordering Information

<b>Standard P506 Models</b>	<b>15P506-00</b>	Quad CAN bus interface, 4 CAN cores, front I/O, for convection cooled systems, -40..+85°C with qualified components
<b>Miscellaneous Accessories</b>	<b>05P000-01</b>	25 mounting screw sets to fix PMC/XMC modules on carrier boards
<b>Software: Linux</b>	This product is designed to work under Linux. See below for potentially available separate software packages from MEN.	
	<b>13Z015-06</b>	MDISS low-level driver sources (MEN) for 16Z029_CAN (MSCAN/Layer2)
	<b>13Z016-06</b>	MDISS driver (MEN) for 16Z029_CAN (CANopen master)
	<b>13Z061-06</b>	MDISS low-level driver sources (MEN) for 16Z061_PWM
<b>Software: Windows®</b>	This product is designed to work under Windows®. See below for potentially available separate software packages from MEN.	
	<b>10Y000-78</b>	Windows® Embedded Standard 7 BSP for F11S, F19P, F21P, F22P, G20, G22, XM1L, XM2, MM1, MM2, SC21, SC24, SC27, BC50M, BC50I, BL50W, BL50S, DC13, F206, F210, F215, F216, G215, P506, P507 and P511
	<b>13P506-77</b>	Windows® Installset (MEN) for P506 (Includes all free drivers developed by MEN for the supported hardware.)
	<b>13Z016-70</b>	MDISS Windows® driver (MEN) for 16Z029_CAN (CANopen master)
<b>Software: VxWorks®</b>	This product is designed to work under VxWorks®. For details regarding supported/unsupported board functions please refer to the corresponding software data sheets.	
	<b>13Z015-06</b>	MDISS low-level driver sources (MEN) for 16Z029_CAN (MSCAN/Layer2)
	<b>13Z016-06</b>	MDISS driver (MEN) for 16Z029_CAN (CANopen master)
	<b>13Z061-06</b>	MDISS low-level driver sources (MEN) for 16Z061_PWM
<b>Software: QNX®</b>	This product is designed to work under QNX®. For details regarding supported/unsupported board functions please refer to the corresponding software data sheets.	
	<b>13Z015-06</b>	MDISS low-level driver sources (MEN) for 16Z029_CAN (MSCAN/Layer2)
	<b>13Z016-06</b>	MDISS driver (MEN) for 16Z029_CAN (CANopen master)
	<b>13Z061-06</b>	MDISS low-level driver sources (MEN) for 16Z061_PWM
For operating systems not mentioned here <a href="#">contact MEN sales</a> .		
<b>Documentation</b>	Compare Chart mezzanine functions on PMC/XMC and PC-MIP® <a href="#">» Download</a>	
	<b>20P506-00</b>	P506 User Manual

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