M199 – FPGA-based USM Main M-Module

- **Main M-Module for USM Universal Submodules**
- **1 USM slot**
- **1 FPGA 33,216 LE (for user-defined I/O and Nios® soft core)**
- **32 MB DDR2 SDRAM**
- **8 MB Flash**
- **-40 to +85°C with qualified components**

USM Universal Submodules make M-Modules more flexible than ever. The main M-Module M199 mezzanine card gets its specific function through the IP cores implemented inside its onboard FPGA. This function can be changed at any time through implementation of different IP cores. The corresponding line drivers are realized on the USM which is simply plugged on the M199.

The same USM may also be used on PMC or XMC and conduction-cooled PMC main modules. A new design is then limited to the USM module and the FPGA content and therefore saves development time and costs. A Nios® soft processor implemented in the Cyclone® II FPGA by Altera® provides local intelligence where needed.

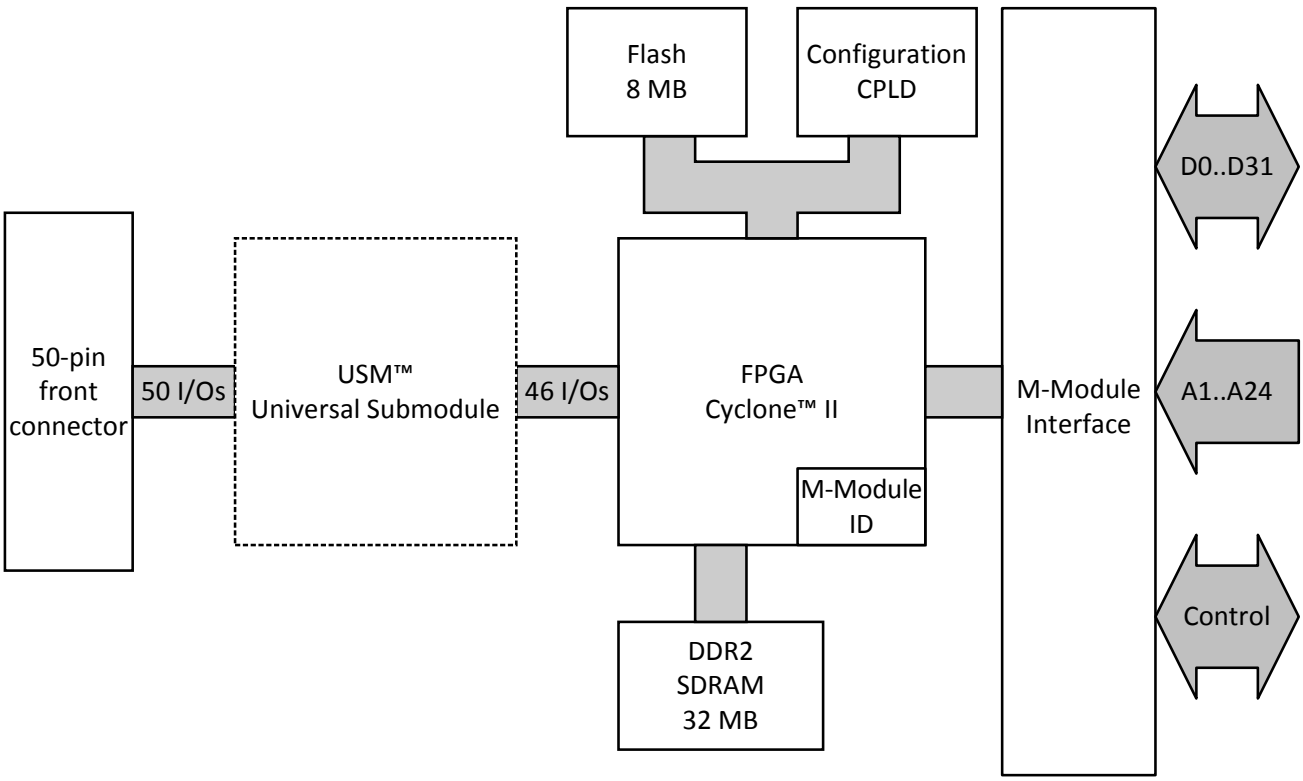
The I/O signals are led to the USM and then to a SCSI connector at the front of the M199.

The growing range of Wishbone-based standard IP cores from MEN comprise different UARTs, Ethernet, fieldbus interfaces, graphics, digital I/O etc. For users who like to write and/or implement specific IP cores on their own a complete FPGA USM development kit is available.

The USM concept has been developed for harsh environments. Therefore, the M199 uses robust connectors to the USM while all other components are soldered, and operates in a -40 to +85 °C temperature range with qualified components.

The M199 is based on the M-Module ANSI mezzanine standard. It can be used as an I/O extension in any type of bus system, i.e. CPCI, VME or on any type of stand-alone SBC. Appropriate M-Module carrier cards in 3U, 6U and other formats are available from MEN or other manufacturers.

Diagram


Flash
8 MB
Configuration
CPLD
D0..D31
50-pin
front
connector
50 I/Os
USM™
Universal Submodule
46 I/Os
FPGA
Cyclone™ II
M-Module
ID
M-Module
Interface
A1..A24
Control
DDR2
SDRAM
32 MB

Technical Data

Functionality	■ User-defined through FPGA ■ Line drivers and/or additional hardware implemented on USM Universal Submodule (not included)
Memory	■ 32MB SDRAM memory □ Soldered □ DDR2 □ 133MHz memory bus frequency □ FPGA-controlled ■ 8MB non-volatile Flash □ 2MB for FPGA data □ 6MB for user data or Nios® firmware □ FPGA-controlled
FPGA	■ Standard factory FPGA configuration: □ Main bus interface □ Altera® SOPC Unit incl. Nios® II/f soft processor, GPIO, UART and DDR2 SDRAM control □ Wishbone-to-Avalon®/Avalon®-to-Wishbone bridges □ Reset controller, interrupt controller, SMBus controller, GPIO controller □ M-Module to Wishbone bridge, ID EEPROM emulation □ 16Z045_FLASH - Flash interface ■ The FPGA offers the possibility to add customized I/O functionality. See FPGA.
USM Slot	■ One slot for a standard USM module ■ For implementation of line drivers and/or additional hardware
Miscellaneous	■ Eight onboard LEDs at bottom side of board, FPGA-controlled □ One used to show FPGA load status, seven free for user-defined functions (GPIO) ■ I²C interface to detect the USM module
M-Module Characteristics	■ Compliant with M-Module standard ■ The actual characteristics implemented depend on the USM module and FPGA function! ■ Prepared for A08, A24, D08, D16, D32, INTA, INTB, INTC, DMA08, DMA16, DMA32, TRIGI, TRIGO, IDENT
Peripheral Connections	■ Via front panel on a shielded 50-pin HP D-Sub SCSI 2 receptacle connector
Electrical Specifications	■ Isolation voltage: □ Voltage depends on implementation and signal routing of USM □ Voltage between the connector shield and isolated ground is limited to approx. 180V using a varistor; AC coupling between connector shield and isolated ground through 47nF capacitor ■ Supply voltage/power consumption: □ +5V (-3%/+5%), 400mA max. (M199 only), 1000mA max. (M199 with USM) ■ MTBF: 533,355h @ 40°C according to IEC/TR 62380 (RDF 2000)
Mechanical Specifications	■ Dimensions: conforming to M-Module standard ■ Weight: 70g (w/o USM module)
Environmental Specifications	■ Temperature range (operation): □ -40..+85°C (qualified components) □ Airflow: min. 10m³/h ■ Temperature range (storage): -40..+85°C ■ Relative humidity (operation): max. 95% non-condensing ■ Relative humidity (storage): max. 95% non-condensing ■ Altitude: -300m to + 3,000m ■ Shock: 15g/11ms ■ Bump: 10g/16ms ■ Vibration (sinusoidal): 2g/10..150Hz ■ Conformal coating on request
Safety	■ PCB manufactured with a flammability rating of 94V-0 by UL recognized manufacturers

Technical Data

EMC	■ Tested according to EN 55022 (radio disturbance), IEC1000-4-2 (ESD) and IEC1000-4-4 (burst)
Software Support	■ Nios® sample design for Quartus® II development tools ■ Flash update tools for Windows®, Linux, VxWorks® ■ Driver software depending on implemented FPGA functions ■ For more information on supported operating system versions and drivers see Downloads.

FPGA

This product offers the possibility to add customized I/O functionality in FPGA.

Flexible Configuration	■ Customized I/O functions can be added to the FPGA. ■ It depends on the board type, pin counts and number of logic elements which IP cores make sense and/or can be implemented. Please contact MEN for information on feasibility. ■ You can find more information on our web page "User I/O in FPGA"
FPGA Capabilities	■ FPGA Altera® Cyclone® II EP2C35 □ 33,216 logic elements □ 483,840 total RAM bits □ Supports Nios® II soft processor ■ Connection □ Functions can be linked to Wishbone or Avalon® bus □ Available pin count: 46 pins (FPGA to USM) □ Functions available via USM at front I/O connector ■ MEN offers an FPGA Development Package as well as Flash update tools for different operating systems.
MEN IP Cores	■ MEN offers a large number of standard IP cores. ■ Examples: □ IDE (e.g. PIO mode 0, UDMA mode 5) □ UARTs □ CAN bus □ Display control □ Fast Ethernet (10/100Base-T) □ ... ■ For IP cores developed by MEN please refer to our IP core overview. □ IP Core compare chart (PDF) ■ MEN also offers development of new (customized) IP cores.
Third-Party IP Cores	■ Third-party IP cores can also be used in combination with MEN IP cores. ■ Examples: □ www.altera.com □ www.opencores.org
FPGA Design Environment	■ Altera® offers free download of Quartus® II Web Edition □ Complete environment for FPGA and CPLD design □ Includes schematic- and text-based design entry □ Integrated VHDL and Verilog HDL synthesis and support for third-party synthesis software □ SOPC Builder system generation software □ Place-and-route, verification, and programming ■ Altera® Quartus® II Web Edition FPGA design tool

Configuration & Options

Standard Configurations

Article No.	I/O Connector	Operation Temperature
04M199-00	50-pin SCSI 2	-40..+85°C

Options

I/O	■ Front Connections □ 25-pin D-Sub receptacle connector instead of 50-pin SCSI 2 connector □ For 25 I/O signals □ For the availability and assignment of I/O signals please see the USM Specification

Please note that some of these options may only be available for large volumes. Please ask our sales staff for more information.

Ordering Information

Standard M199 Models	**04M199-00**	USM main M-Module, -40..85°C with qualified components
Related Hardware	**19M199-00**	M-Module USM FPGA development kit consisting of 1 FPGA-based universal M-Module M199, 1 bare USM Universal Submodule US0, 1 eval board AD99 for USM/FPGA development, 1 SA-Adapter SA1 (RS232), connection cable, FPGA/Nios® example project including M-Module core (key for download), 0..+60°C
Miscellaneous Accessories	**05P599-00**	PMC/M-Module cable, 2m, with 50-pin HP D-Sub 50 M both sides, 0..+60°C
	08US00-00	Universal Submodule for prototyping, -40..+85°C qualified
Software: FPGA	**16M199-00**	Nios® M-Module USM FPGA Development Package (MEN) (without Altera® Quartus® II) (license included in M-Module USM FPGA Development Kit)
Software: Linux	This product is designed to work under Linux. See below for potentially available separate software packages from MEN.	
	13M199-06	MDIS5 low-level driver sources (MEN) for M199
	13Z100-91	Linux FPGA update tool (MEN)
Software: Windows®	This product is designed to work under Windows®. See below for potentially available separate software packages from MEN.	
	13M199-70	MDIS4/2004 / MDIS5 Windows® driver (MEN) for M199
	13Y018-70	Windows® 64-bit FPGA update tool (MEN)
Software: VxWorks®	This product is designed to work under VxWorks®. For details regarding supported/unsupported board functions please refer to the corresponding software data sheets.	
	13M199-06	MDIS5 low-level driver sources (MEN) for M199
	13Z100-60	VxWorks® FPGA update tool (MEN)
Software: QNX®	This product is designed to work under QNX®. For details regarding supported/unsupported board functions please refer to the corresponding software data sheets.	
	13M199-06	MDIS5 low-level driver sources (MEN) for M199
	13Z100-40	QNX® FPGA update tool (MEN)

For operating systems not mentioned here contact MEN sales.

Documentation	**20M199-00**	M199 User Manual
	20US00-00	USM Specification
	21M199-00	P599/M199 Programmer's Guide

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