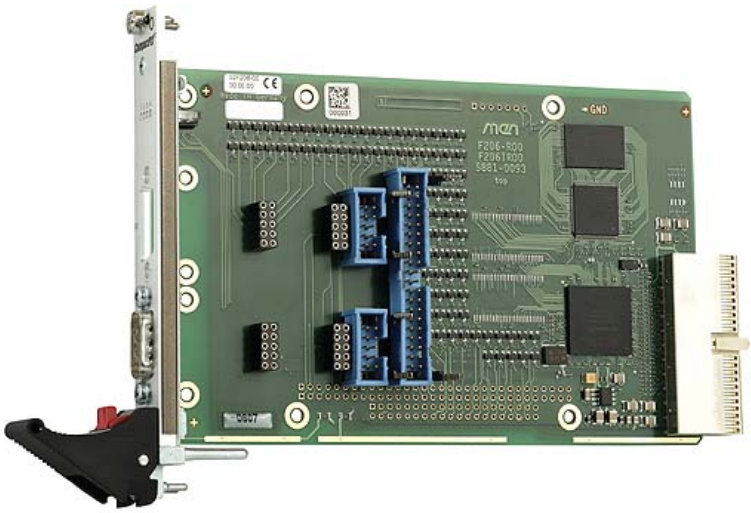
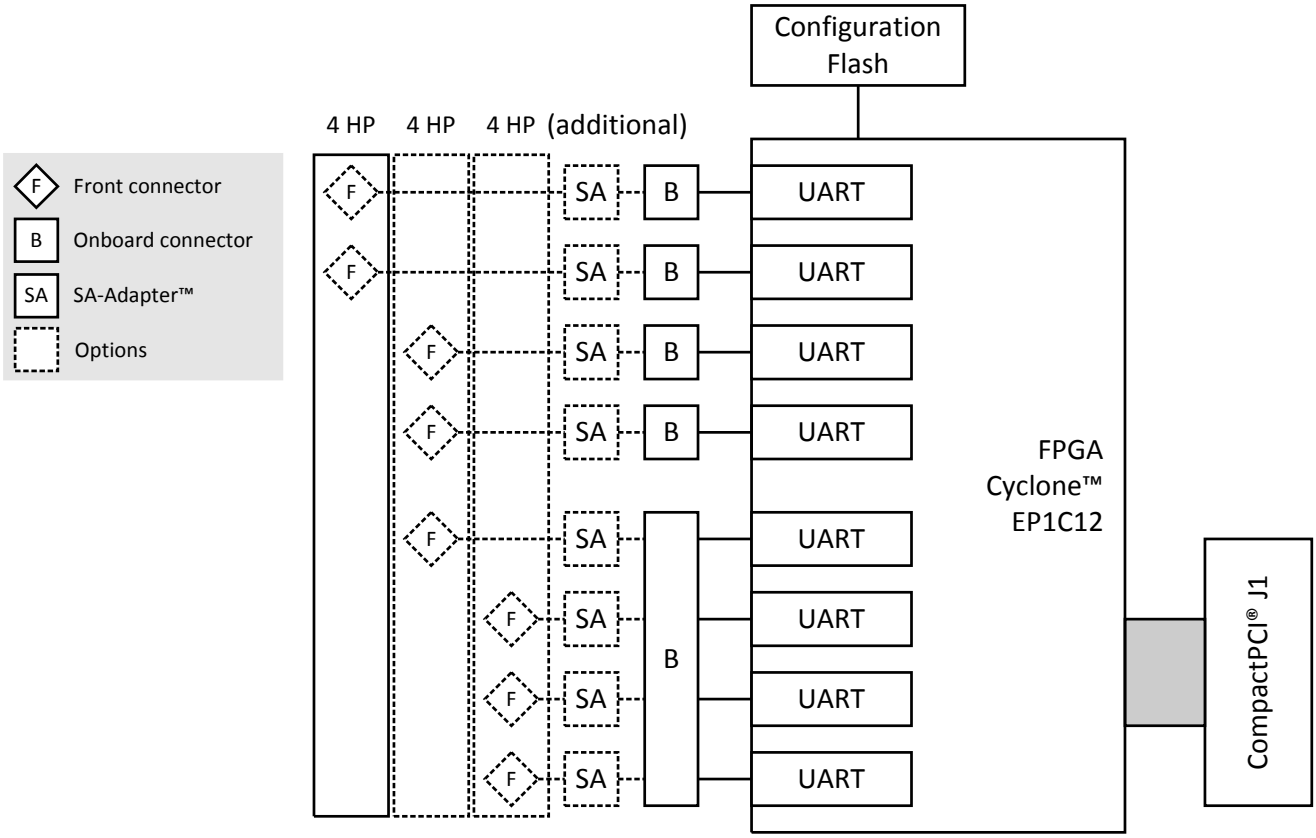
# F206 – 3U CompactPCI® Octal UART for RS232, RS422, RS485

- **Octal 16450 UART**
- **RS232/RS422/RS485, isolated/not isolated**
- **Physical layer via SA-Adapters™**
- **Large receive and transmit FIFOs**
- **Very high data rates up to 2 Mbit/s**
- **Full handshake support**
- **Hardware flow control for RS485 half duplex**
- **Also for other protocols like HDLC**
- **-40 to +85°C with qualified components**



The F206 is a universal octal UART based on 3U CompactPCI®. The physical layer can be realized individually for each channel by means of SA-Adapters™.
SA-Adapters™ are small universal boards providing the physics for legacy serial I/O, fieldbus interfaces and other small I/O functions. Most SA-Adapters™ use 9-pin D-Sub connectors which are accessible at the front panel. Alternatively, the adapter can be connected to the front panel via ribbon cable. The SA concept allows to add additional I/O interfaces to the F206, enhancing flexibility with regard to the line transceivers and isolation requirements.
Two SA-Adapters™ can be mounted directly on the F206 (single-slot solution), the other maximum six adapters need more front-panel space and are connected to the carrier via ribbon cable. Especially useful adapters for the F206 are isolated and non-isolated adapters for RS232, RS422 and RS485 interfaces. Different types can be used on one F206.
The octal UART is realized by means of an FPGA. The register set is fully 16450 compatible, even with larger, 60-byte FIFOs.
The FPGA is loaded automatically after power-up from a 2-MB standard NOR Flash device. It is also possible to access this Flash from the CompactPCI® bus to update its contents. There is a primary and a secondary FPGA filling in the Flash. Normally just the secondary code is used. Only in case of a fault during the update process the primary contents allow another update of the Flash from the CompactPCI® bus.
Optionally also 16 MB SDRAM can be installed to complement the functions of the FPGA. This DRAM can be used for example as a large buffer memory for more complex protocols.
The F206 is designed for use in rugged environments. For example, all components are specified for an operating temperature of -40 to +85°C.

# Diagram


Configuration Flash
4 HP
4 HP
4 HP (additional)
F Front connector
B Onboard connector
SA SA-Adapter™
Options
F
SA
B
UART
FPGA Cyclone™ EP1C12
CompactPCI® J1

# Technical Data

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| **UARTs** | ■ Up to eight UARTs<br>■ Accessible via onboard connectors<br>■ Physical interface at front panel using SA-Adapters™ via 10-pin ribbon cable<br>■ Different variations with SA-Adapters™ possible:<br>□ RS232<br>□ RS422<br>□ RS485<br>■ Data rates up to 2 Mbit/s<br>■ 60-byte transmit/receive buffer<br>■ Handshake lines: full support; lines depend on SA-Adapters™ |
| **FPGA** | ■ Standard factory FPGA configuration:<br>□ Main bus interface<br>□ 16Z054_SYSTEM - System unit<br>□ 16Z025_UART - UART controller (controls four UARTs)<br>□ 16Z025_UART - UART controller (controls four UARTs)<br>□ 16Z045_FLASH - Flash interface<br>■ The FPGA offers the possibility to add customized I/O functionality. See FPGA.<br>■ Option matrix showing possible IP cores and SA-Adapters™ (PDF) |
| **Miscellaneous** | ■ Four status LEDs |
| **Local PCI Bus** | ■ 32-bit/33-MHz, 3.3 V V(I/O)<br>■ Compliant with PCI Specification 2.2 |
| **CompactPCI® Bus** | ■ Compliance with CompactPCI® Core Specification PICMG 2.0 R3.0<br>■ Peripheral slot<br>■ V(I/O): +3.3 V |
| **Electrical Specifications** | ■ Supply voltage/power consumption:<br>□ +5 V (-3%/+5%), current depends only on mounted SA-Adapters™<br>□ +3.3 V (-3%/+5%), > 500 mA typ. |
| **Mechanical Specifications** | ■ Dimensions: conforming to CompactPCI® specification for 3U boards<br>■ Single 3U front panel slot for up to two UARTs<br>■ Up to two supplementary front panel slots required for overall eight UARTs<br>■ Front panel: aluminum with 1 handle<br>■ Weight: 95 g |
| **Environmental Specifications** | ■ Temperature range (operation):<br>□ -40..+85°C (qualified components)<br>□ Airflow: min. 1.0 m/s<br>■ Temperature range (storage): -40..+85°C<br>■ Relative humidity (operation): max. 95% non-condensing<br>■ Relative humidity (storage): max. 95% non-condensing<br>■ Altitude: -300 m to +3000 m<br>■ Shock: 15 g, 11 ms (EN 60068-2-27)<br>■ Bump: 10 g, 16 ms (EN 60068-2-29)<br>■ Vibration (sinusoidal): 1 g, 10 Hz - 150 Hz (EN 60068-2-6)<br>■ Conformal coating on request |
| **MTBF** | ■ 308 000 h @ 40°C (derived from MIL-HDBK-217F) |
| **Safety** | ■ PCB manufactured with a flammability rating of 94V-0 by UL recognized manufacturers |
| **EMC** | ■ Tested according to EN 55022 (radio disturbance), IEC 61000-4-2 (ESD) and IEC 61000-4-4 (burst) |
| **Software Support** | ■ Driver software for Windows®, Linux, VxWorks®, QNX®<br>■ Flash update tools for Windows®, Linux, VxWorks®<br>■ For more information on supported operating system versions and drivers see Downloads. |

# FPGA

**This product offers the possibility to add customized I/O functionality in FPGA.**

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| **Flexible Configuration** | ■ Customized I/O functions can be added to the FPGA.<br>■ It depends on the board type, pin counts and number of logic elements which IP cores make sense and/or can be implemented. Please contact MEN for information on feasibility.<br>■ You can find more information on our web page "User I/O in FPGA" |
| **FPGA Capabilities** | ■ FPGA Altera® Cyclone® EP1C12<br>□ 12 060 logic elements<br>□ 239 616 total RAM bits<br>■ For UART functions<br>■ 2 MB Flash for FPGA configurations<br>■ Connection<br>□ Total available pin count: 64 pins<br>□ Functions available via onboard I/O connectors<br>□ SA-Adapters™ are used to realize the physical lines.<br>■ Functional updates via software<br>□ MEN offers Flash update tools for different operating systems. |

# Configuration & Options

## Standard Configurations

| Article No. | No. of UARTs | Front Panel | FPGA Cores | Operating Temperature |
|---|---|---|---|---|
| 02F206-00 | 2 (via SA-Adapters) | 4 HP, 2 D-Sub | 8 UARTs | -40..+85°C |
| 02F206-00 + 05F206-02 | 5 (via SA-Adapters) | 8 HP, 5 D-Sub | 8 UARTs | -40..+85°C |
| 02F206-00 + 05F206-03 | 8 (via SA-Adapters) | 12 HP, 8 D-Sub | 8 UARTs | -40..+85°C |

## Options

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| **Physical Layers** | ■ Via up to eight SA-Adapters™<br>■ Different variations possible through FPGA IP cores and SA-Adapters™:<br>□ RS232<br>□ RS422<br>□ RS485<br>□ IBIS master/slave<br>□ CAN bus<br>□ HDLC<br>□ Binary I/O<br>□ InterBus-S<br>□ GPS<br>□ Other physical layers dependent on FPGA configuration<br>□ Option matrix showing possible IP cores and SA-Adapters™ (PDF) |
| **Mechanical** | ■ 4, 8 or 12 HP front panel dependent on number of SA-Adapters™<br>□ 4 HP with 2 onboard SA-Adapters™<br>□ 8 HP with 5 SA-Adapters™<br>□ 12 HP with 8 SA-Adapters™<br>■ One-piece front panel<br>■ Different front panel cut-outs possible |
| **Cooling Concept** | ■ Also available with conduction cooling in MEN CCA frame |

**Please note that some of these options may only be available for large volumes. Please ask our sales staff for more information.**

# Ordering Information

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| **Standard F206 Models** | **02F206-00** | 4 HP FPGA-based UART interface for direct connection of 2 UARTs (2 SA-Adapters™ to be ordered separately) at front, 8 UARTs standard FPGA content plus space for user-defined functions, -40..+85°C with qualified components |
| **SA-Adapters™** | You can find a more detailed overview of possible carrier board/SA-Adapter™ combinations along with software support in our option matrix (PDF). | |
| | **08SA01-00** | RS232, not optically isolated, 0..+60°C |
| | **08SA02-00** | RS422/485, half duplex, optically isolated, 0..+60°C |
| | **08SA02-01** | RS422/485, full duplex, optically isolated, 0..+60°C |
| | **08SA02-07** | RS422/485, full duplex, optically isolated, -40..+85°C screened |
| | **08SA03-00** | 1 RS232, optically isolated, 0..+60°C |
| | **08SA03-01** | 1 RS232, optically isolated, -40..+85°C screened |
| | **08SA08-01** | CAN ISO high-speed, optically isolated, -40..+85°C screened |
| | **08SA15-00** | 8 digital I/O channels, -40..+85°C with qualified components, no RoHS |
| | **08SA22-00** | IBIS master SA-Adapter™, -40..+85°C screened |
| | **08SA22-01** | IBIS slave SA-Adapter™, -40..+85°C screened |
| | **08SA25-00** | GPS receiver, isolated, -40..+85°C screened |
| **Miscellaneous Accessories** | **05F206-02** | Kit (4 HP front panel and cables) for connection of 3 additional UART SA-Adapters™ to F206 and F206N - SA-Adapters™ to be ordered separately (cannot be combined with 05F206-03) |
| | **05F206-03** | Kit (8 HP front panel and cables) for connection of 6 additional UART SA-Adapters™ to F206, F206N - SA-Adapters™ to be ordered separately (cannot be combined with 05F206-02) |
| **Software: Linux** | This product is designed to work under Linux. See below for potentially available separate software packages from MEN. | |
| | **13Z017-06** | MDIS5™ low-level driver sources (MEN) for 16Z034_GPIO, 16Z037_GPIO and 16Z127_GPIO |
| | **13Z025-90** | Linux native driver (MEN) for 16Z025_UART, 16Z057_UART and 16Z125_UART |
| | **13Z055-90** | Linux native driver (MEN) for 16Z055_HDLC with TCP/PPP support |
| | **13Z100-91** | Linux FPGA update tool (MEN) |
| **Software: Windows®** | This product is designed to work under Windows®. See below for potentially available separate software packages from MEN. | |
| | **10Y000-78** | Windows® Embedded Standard 7 BSP for F11S, F19P, F21P, F22P, F75P, G20, G22, XM1L, XM2, MM1, MM2, SC21, SC24, SC27, BC50M, BC50I, BL50W, BL50S, DC13, F206, F210, F215, F216, G215, P506, P507 and P511 |
| | **13F206-70** | Windows® Installset (MEN) for F206<br>(Includes all free drivers developed by MEN for the supported hardware.) |
| | **13Z100-70** | Windows® FPGA update tool (MEN) |

# Ordering Information

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| **Software: VxWorks®** | This product is designed to work under VxWorks®. For details regarding supported/unsupported board functions please refer to the corresponding software data sheets. | |
| | **13Z017-06** | MDIS5™ low-level driver sources (MEN) for 16Z034_GPIO, 16Z037_GPIO and 16Z127_GPIO |
| | **13Z025-60** | VxWorks® native driver (MEN) for 16Z025_UART, 16Z057_UART and 16Z125_UART |
| | **13Z100-60** | VxWorks® FPGA update tool (MEN) |
| **Software: QNX®** | This product is designed to work under QNX®. For details regarding supported/unsupported board functions please refer to the corresponding software data sheets. | |
| | **13Z017-06** | MDIS5™ low-level driver sources (MEN) for 16Z034_GPIO, 16Z037_GPIO and 16Z127_GPIO |
| | **13Z025-40** | QNX® 6.3 native driver (MEN) for 16Z025_UART and 16Z125_UART |
| | **13Z025-41** | QNX® 6.4 native driver (MEN) for 16Z025_UART and 16Z125_UART |
| | **13Z025-42** | QNX® 6.5 native driver (MEN) for 16Z025_UART and 16Z125_UART |
| | **13Z100-40** | QNX® FPGA update tool (MEN) |

**For operating systems not mentioned here contact MEN sales.**

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| **Documentation** | Compare Chart 3U CompactPCI® / PlusIO CPU cards » Download | |
| | Compare Chart 3U CompactPCI® / PlusIO peripheral cards » Download | |
| | **20F206-00** | F206 User Manual |
| | **20SA01-00** | SA1 User Manual |
| | **20SA02-00** | SA2 User Manual |
| | **20SA03-00** | SA3 User Manual |
| | **20SA08-00** | SA8 User Manual |
| | **20SA15-00** | SA15 User Manual |
| | **20SA22-00** | SA22 User Manual |
| | **20SA25-00** | SA25 User Manual |
| | **22Z025-ER** | 16Z025_UART Errata |

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